5th ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)

September 11-13, 2023 Snowbird, Utah

Program Papers

Registration: Cottonwood Lobby; Meeting room for all sessions: Cottonwood B; Lunch and Dinner room: Cottonwood A

Sun., Sept. 10, 2023	
18:30-21:00	**Reception (**Seven Summits room)
Mon., Sept. 11, 2023	
08:30-08:40	**Welcome**
08:40-09:25	**Keynote: Analog Synthesis 3.0: AI/ML to Synthesize and Test Analog ICs: Hope or Hype?** **Georges Gielen** - KU Leuven Moderator: Hussam Amrouch - Technical University of Munich
09:25-09:55	**Break**
09:55-11:10	**Session 1: LLMs and GNNs for EDA** Session Chair: Youngsoo Shin - Korea Advanced Institute of Science and Technology **Chip-Chat: Challenges and Opportunities in Conversational Hardware Design** **Jason Blocklove**, Siddharth Garg, Ramesh Karri - New York University Hammond Pearce - University of New South Wales **ChatEDA: A Large Language Model Powered Autonomous Agent for EDA** Zhuolun He - The Chinese University of Hong Kong Haoyuan Wu - Shanghai Artificial Intelligent Laboratory Xinyun Zhang, Xufeng Yao, Su Zheng - The Chinese University of Hong Kong Haisheng Zheng - Shanghai Artificial Intelligent Laboratory **Bei Yu** - The Chinese University of Hong Kong **Characterize the Ability of GNNs in Attacking Logic Locking** **Wei Li**, Ruben Purdy, Jose Moura, Shawn Blanton - Carnegie Mellon University
11:10-11:25	**Break**
11:25-12:40	**Session 2: Early Prediction of Circuit Performance using ML** Session Chair: Bei Yu - The Chinese University of Hong Kong

	ASAP: Accurate Synthesis Analysis and Prediction with Multi-Task Learning Yikang Ouyang - The Hong Kong University of Science and Technology (Guangzhou) Sicheng Li - Alibaba Group **Dongsheng Zuo**, Hanwei Fan, Yuzhe Ma - The Hong Kong University of Science and Technology (Guangzhou) **Using Graph Neural Networks for Timing Estimations of RTL Intermediate Representations** **Daniela Sanchez Lopera**, Ishwor Subedi, Wolfgang Ecker - Infineon Technologies AG **Early Identification of Timing Critical RTL Components using ML based Path Delay Prediction** Prianka Sengupta, Aakash Tyagi - Texas A&M University Yiran Chen - Duke University **Jiang Hu** - Texas A&M University
12:40-13:40	**Lunch**
13:40-14:25	**Plenary: Beyond Hyperparameter Optimization: Using AI to address Digital Implementation Challenges** **Chuck Alpert** - Cadence Design Systems Moderator: Jiang Hu - Texas A&M University
14:25-14:40	**Break**
14:40-15:55	**Session 3: MLCAD Infrastructure and Industry Application** Session Chair: Rajeev Jain - Qualcomm **(Invited) Shared Infrastructure for MLCAD** **Jiang Hu** - Texas A&M University **(Invited) APEX: Recommending Design Flow Parameters Using a Variational Autoencoder** **Michael Kazda**, Michael Monkowski, George Antony - IBM **Optimizing Constrained Random Verification with ML and Bayesian Estimation** **Bhuvnesh Kumar**, Ganapathy Parthasarathy, Saurav Nanda, Sridhar Rajakumar - Synopsys Inc.
15:55-16:10	**Break**
16:10-17:50	**Session 4: ML for Analog Design** Session Chair: Paul Franzon - North Carolina State University

	MMM: Machine Learning-Based Macro-Modeling for Linear Analog ICs and ADC/DACs **Yishuang Lin**, Yaguang Li - Texas A&M University Meghna Madhusudan, Sachin Sapatnekar, Ramesh Harjani - University of Minnesota Jiang Hu - Texas A&M University **Hybrid Utilization of Subgraph Isomorphism and Relational Graph Convolutional Networks for Analog Functional Grouping Annotation** **Zhengfeng Wu** - Drexel University Isabel Song - University of Pennsylvania Ioannis Savidis - Drexel University **Differentiable Neural Network Surrogate Models for gm/ID-based Analog IC Sizing Optimization** **Yannick Uhlmann**, Till Moldenhauer, Jürgen Scheible - Reutlingen University **Machine Learning-based Fast Circuit Simulation for Analog Circuit Array** Jaeseung Lee, Sejin Park, Minhyuk Kweon, **Seokhyeong Kang** - Pohang University of Science and Technology
17:50-18:20	**Break**
18:20-20:50	**Dinner and Panel: Generative AI in EDA** **Yiyu Shi** - University of Notre Dame, **Stelios Diamantidis** - Synopsys Inc., **Norman Chang** - ANSYS, Inc., **Haoxing "Mark" Ren** - NVIDIA Moderator: Marilyn Wolf - University of Nebraska-Lincoln
Tue., Sept. 12, 2023	
08:30-09:15	**Keynote: ML-augmented Simulation and Co-optimization for Semiconductor Applications and Design Workflows** **Norman Chang** - ANSYS, Inc. Moderator: Andrew B. Kahng - University of California at San Diego
09:15-09:30	**Break**
09:30-10:45	**Session 5: International MLCAD Activities** Session Chair: Siddharth Garg - New York University **(Invited) AI-EDA: Toward a Holistic Approach to AI-Powered EDA** **Youngsoo Shin** - Korea Advanced Institute of Science and Technology

	(Invited) ML-TCAD: Perspectives and Challenges on Accelerating Transistor Modeling using ML Rodion Novkin, Simon Thomann, **Hussam Amrouch** - Technical University of Munich **(Invited) From Theory to Practice: Advancements & Challenges in Security of Machine Learning for EDA** Jingyu Pan, Chen-Chia Chang, **Guanglei Zhou** - Duke University Jiang Hu - Texas A&M University Yiran Chen - Duke University
10:45-11:00	**Break**
11:00-12:15	**Session 6: ML for Verification** Session Chair: Marilyn Wolf - University of Nebraska-Lincoln **NeuroPDR: Integrating Neural Networks in the PDR Algorithm for Hardware Model Checking** **Guangyu Hu**, Wei Zhang - The Hong Kong University of Science and Technology Hongce Zhang - The Hong Kong University of Science and Technology (Guangzhou) **DepthGraphNet: Circuit Graph Isomorphism Detection via Siamese-Graph Neural Networks** **Fin Amin**, Soumyadeep Chatterjee, Paul Franzon - North Carolina State University **ConVERTS: Contrastively Learning Structurally InVariant Netlist Representations** **Animesh Basak Chowdhury**, Jitendra Bhandari, Luca Collini, Ramesh Karri - New York University Benjamin Tan - University of Calgary Siddharth Garg - New York University
12:15-13:15	**Lunch**
13:15-14:00	**Plenary: Machine Learning in EDA: When and How** **Bei Yu** - The Chinese University of Hong Kong Moderator: Jiang Hu - Texas A&M University
14:00-14:15	**Break**
14:15-15:30	**Session 7: ML for Routability** Session Chair: Vidya A. Chhabria - Arizona State University **Routability-Driven Power Distribution Network Synthesis with IR-Drop Budgeting**

	Wonjae Lee, Insu Cho, Gangmin Cho, Youngsoo Shin - Korea Advanced Institute of Science and Technology **Simultaneous Clock Wire Sizing and Shield Insertion for Minimizing Routing Blockage** **Yoonsang Song**, Gangmin Cho, Wonjae Lee, Youngsoo Shin - Korea Advanced Institute of Science and Technology **A Robust Routing Guide Generation Approach for Mixed-Size Designs** Zhi-Hong Lee, Chen-Han Lu, Hsin-Hung Pan, **Ting-Chi Wang** - National Tsing Hua University Po-Yuan Chen, Chin-Fang Cindy Shen - Synopsys Taiwan Co., Ltd.
15:30-15:45	**Break**
15:45-17:15	**Generative AI for Silicon Design: Hands-on Session Presented by Synopsys**
17:15-19:30	**Social Event** (16:30 - 18:30: Mountain Coaster open; 17:15 - 19:30: Tram open)
19:30-21:30	**Dinner**
Wed., Sept. 13, 2023	
08:30-09:15	**1st MLCAD Contest: IEEE/ACM MLCAD 2023 FPGA Macro-Placement Contest** **Ismail Bustany -** AMD
09:15-09:30	**Break**
09:30-10:15	**Keynote: Bridging Divides: Unifying AI Architectures from Edge to Cloud** **Ivo Bolsens –** AMD Moderator: Rajeev Jain - Qualcomm
10:15-10:30	**Break**
10:30-12:30	**Embedded Tutorial on EDA using Large Language Models** Shailja Thakur, Jason Blocklove, Siddharth Garg, Hammond Pearce
12:30-12:40	**Closing Remarks** (Box lunch available)